

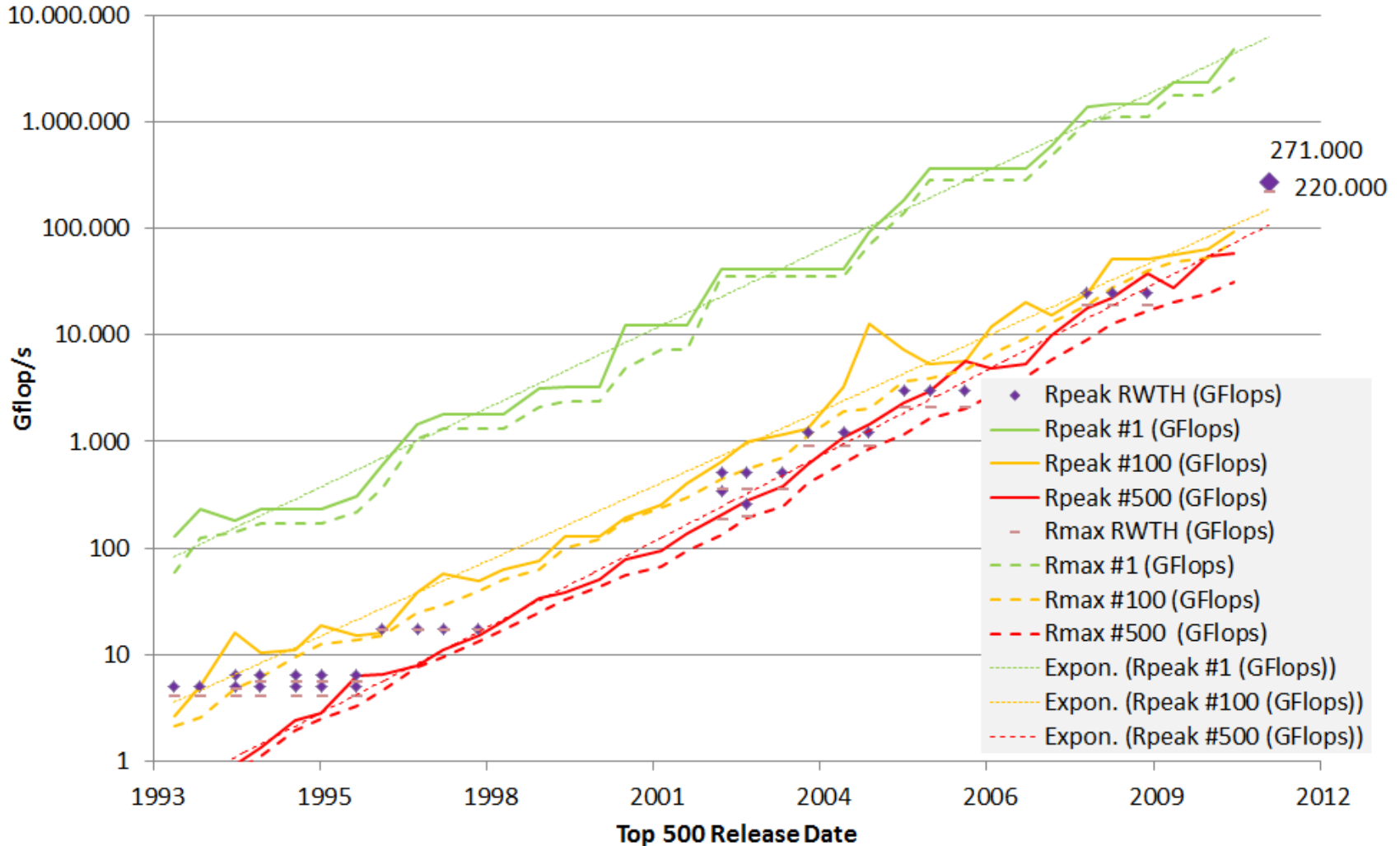
# Parallel Programming Summer Course 2013

## Introduction

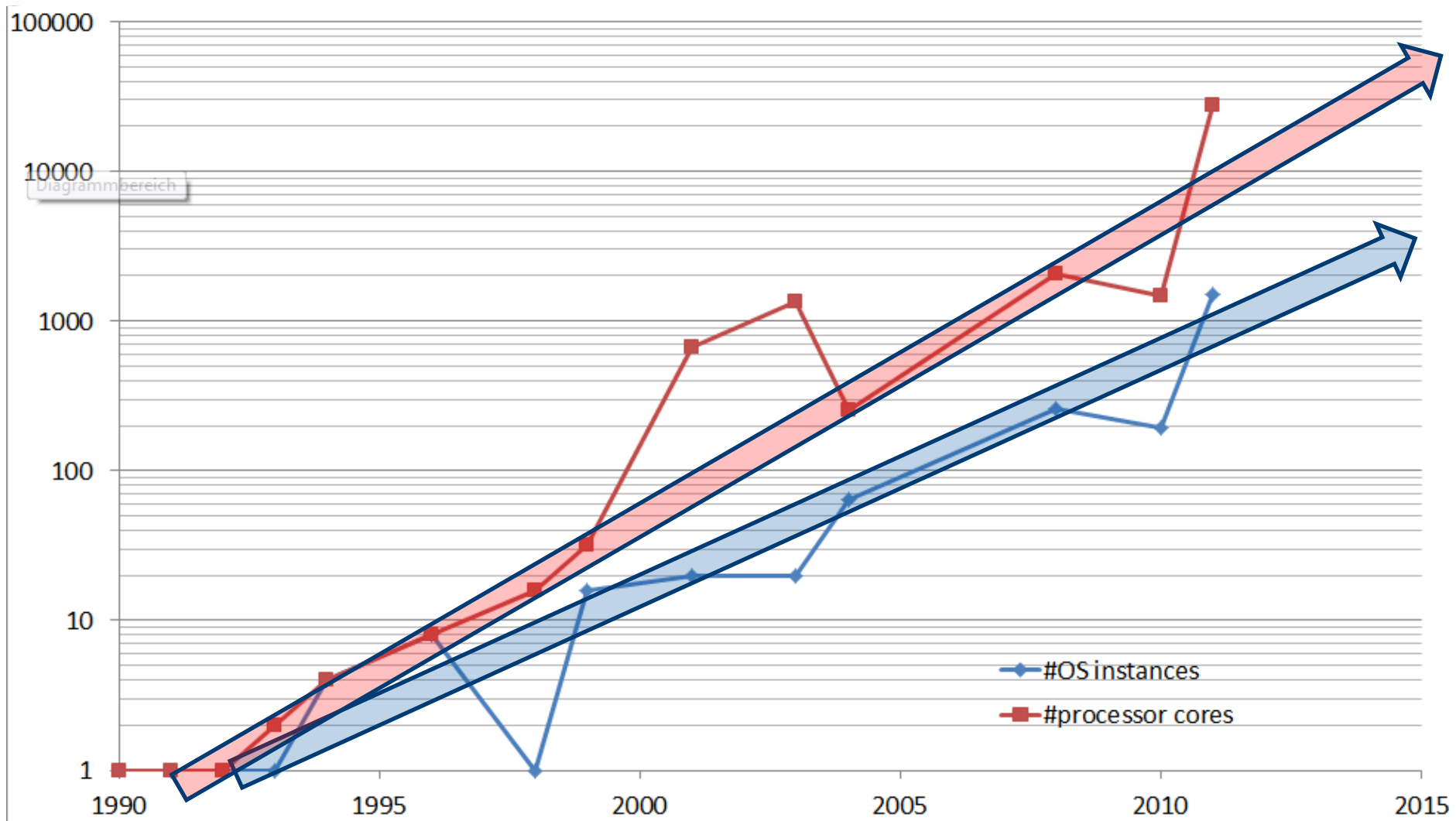
*Dieter an Mey*

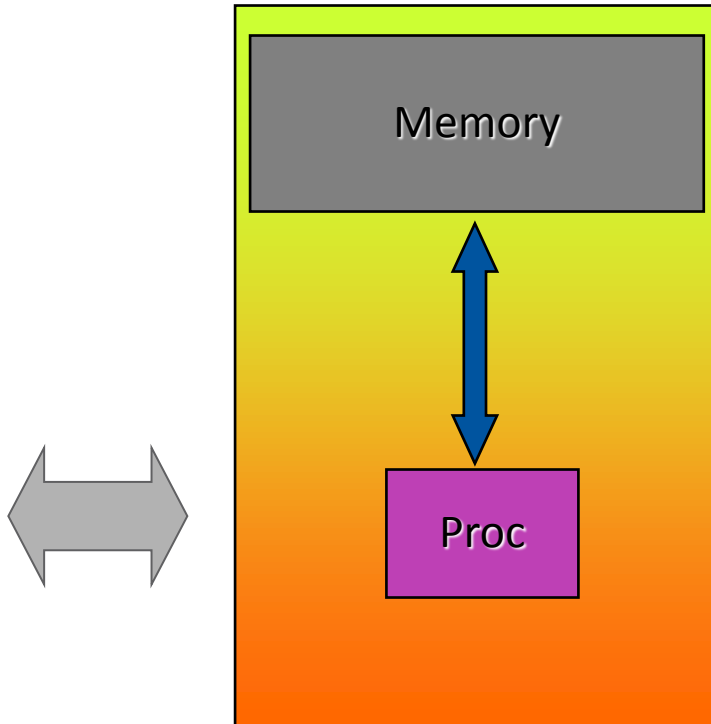
*Center for Computing and Communication*

RWTH Systems in Top500 List over Time



# Growth of #OS instances / #processor cores





Main memory to store data and programs.

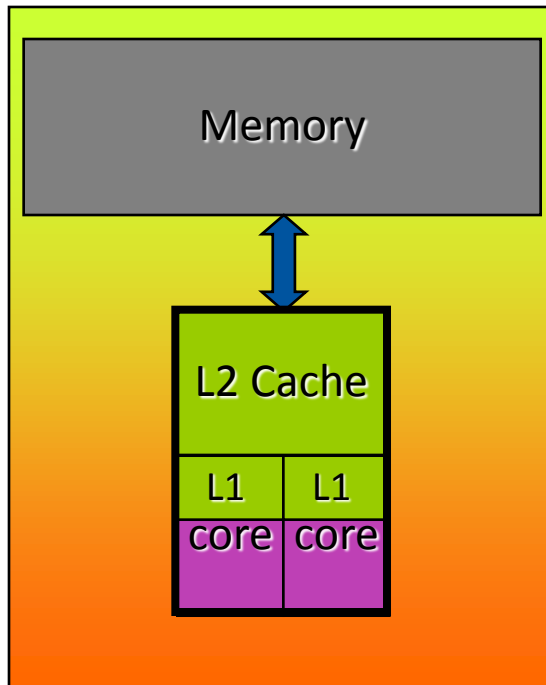
Processor to fetch program from memory, and execute program instructions:  
Load data from memory, process data and write results back to memory.

Accessing memory takes time.

Today memory bandwidth and latency frequently is a severe bottleneck!

Input/ output  
is not covered here.

# Computer Architecture: Refined View with Multiple Cache Levels



Since 2005/6 Intel and AMD are producing dualcore processors for the mass market.

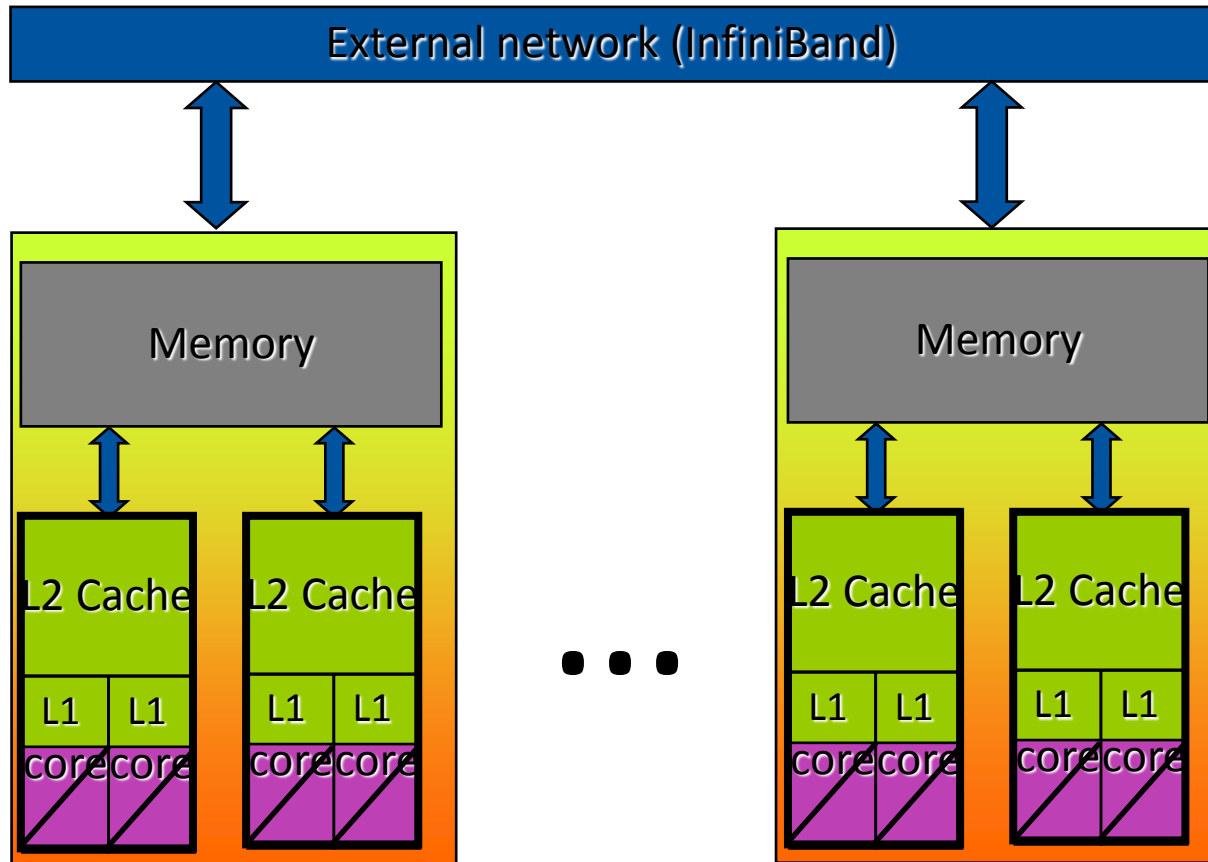
Today multicores are ubiquitous.

Currently 4 to 16 cores per chip are quite common.

Caches have been employed since long to remedy the memory bottleneck to a certain degree.

But with a growing number of cores, the memory bottleneck is still growing !

## ■ Cluster of Multiprocessor Nodes with Multicore Processors

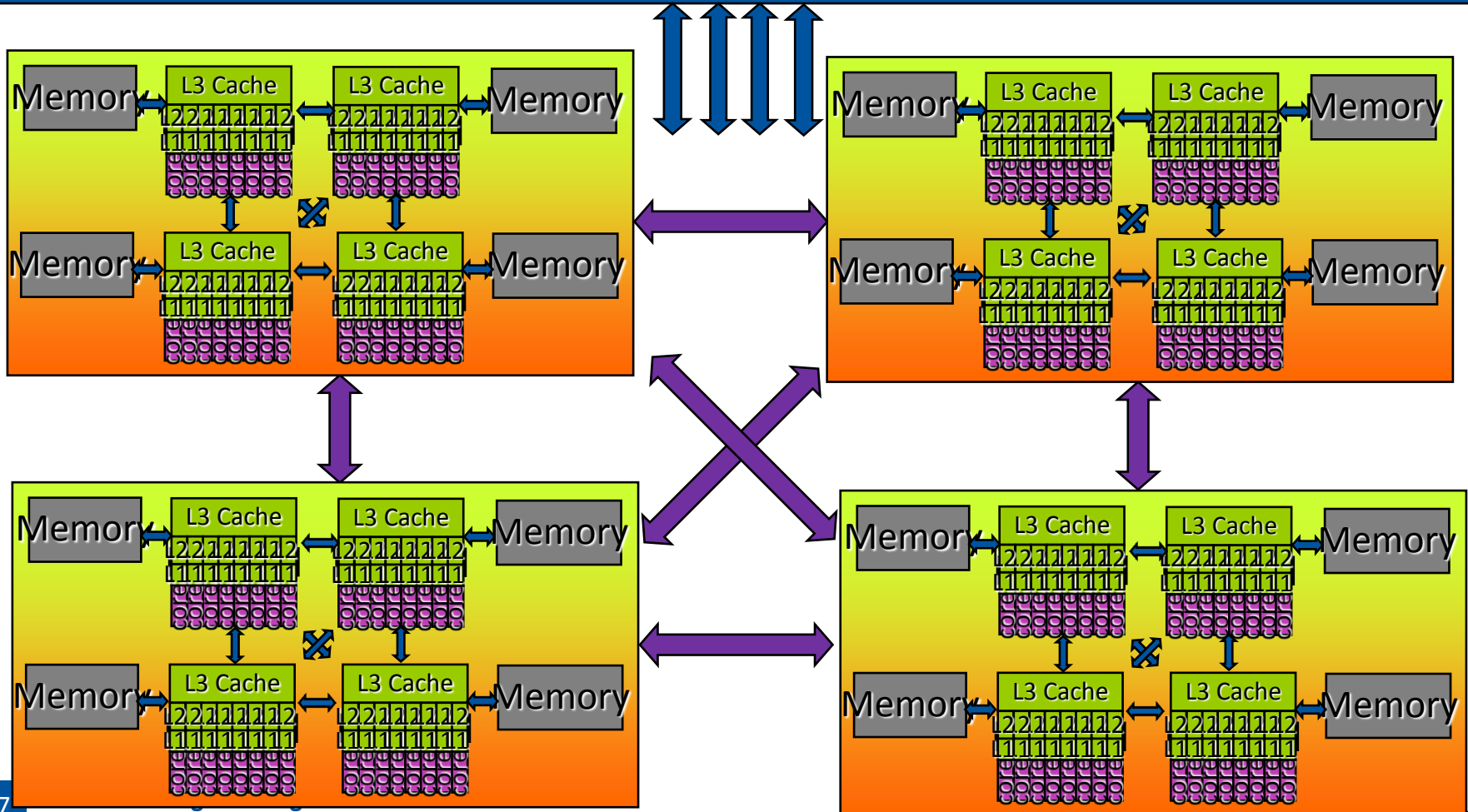


For High Performance Computing (HPC) large clusters of many nodes with multiple multicore processors are connected by fast networks like InfiniBand.

Each node is a shared memory parallel computer where all cores of all processors have access to one main memory.

■ Bull BCS System

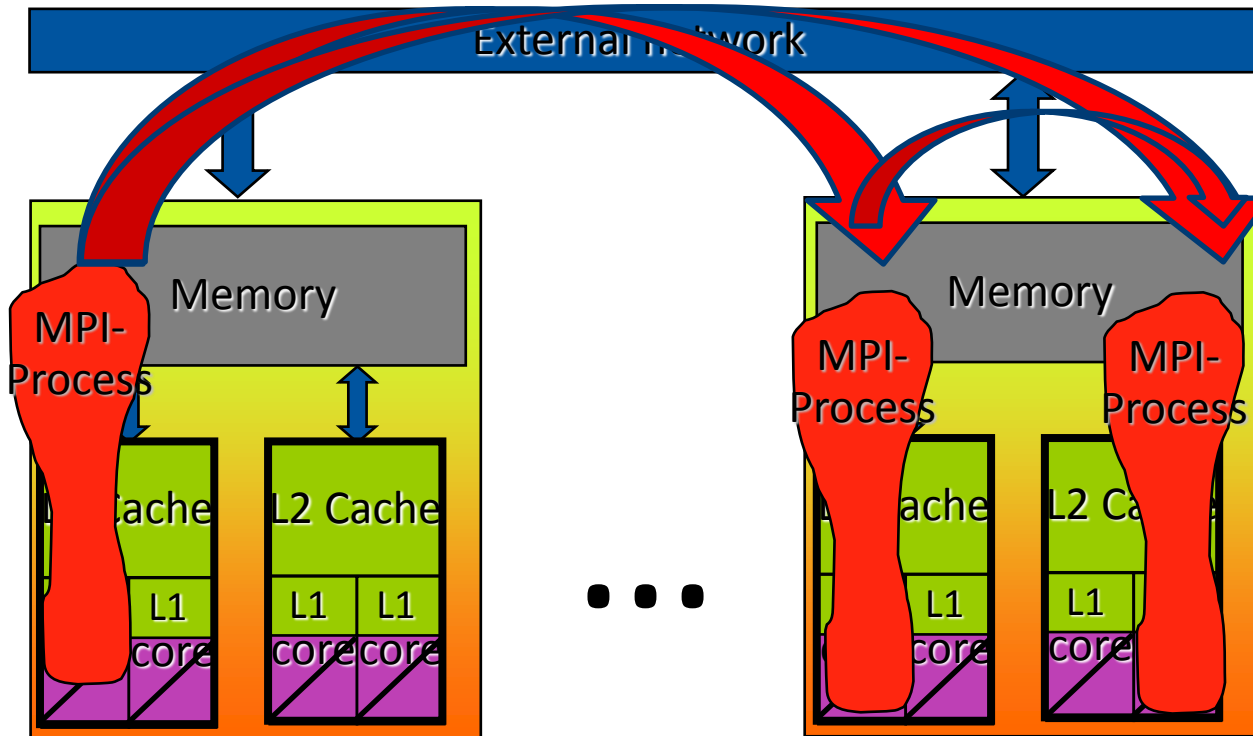
InfiniBand Network



# Message Passing with MPI

## On Distributed Memory Parallel Computers

Typically, when using Message Passing with MPI, one MPI process runs on each processor core



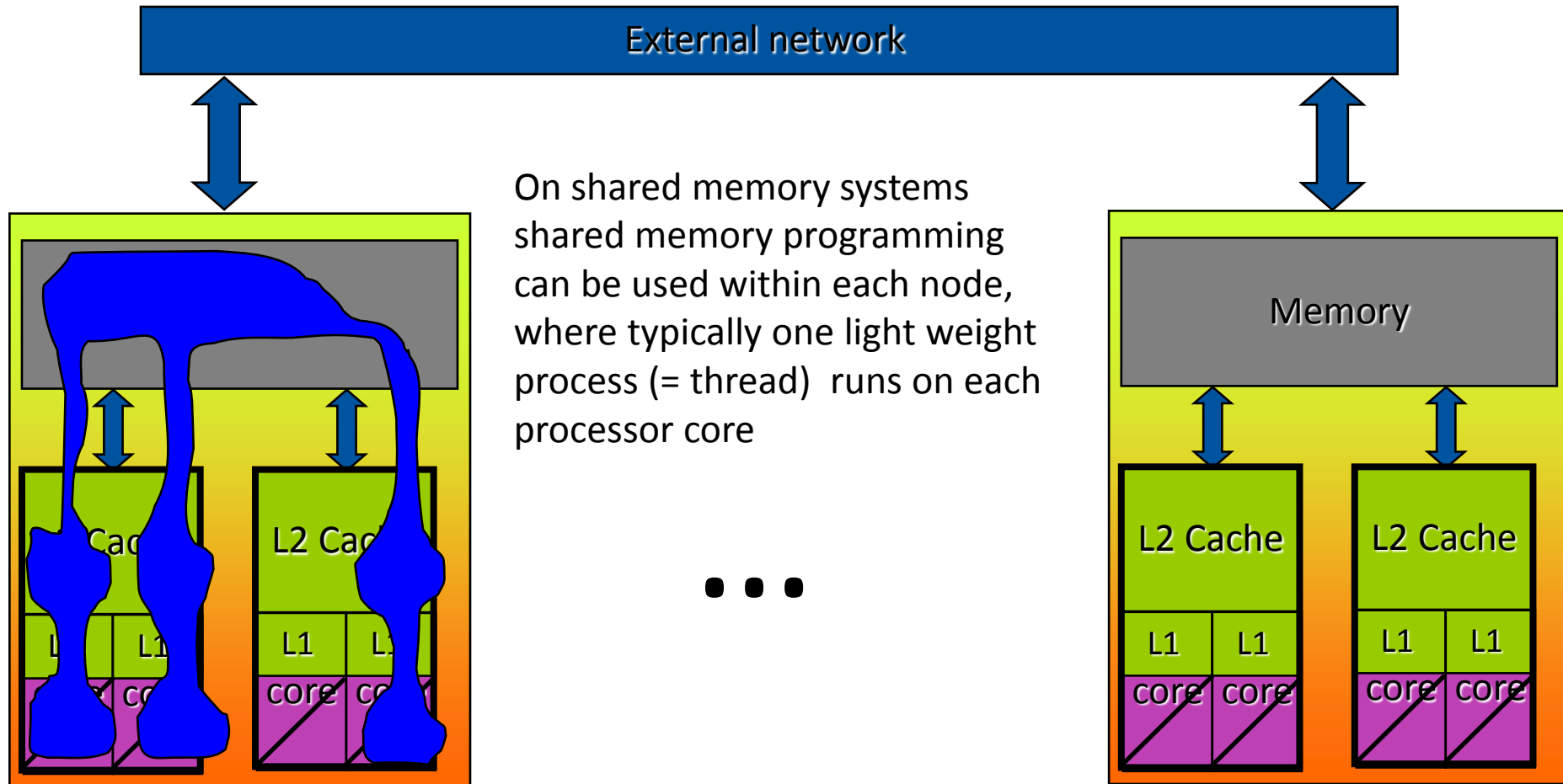
MPI is the de-facto standard for message passing.

MPI is a program library plus a mechanism to launch multiple cooperating executable programs.

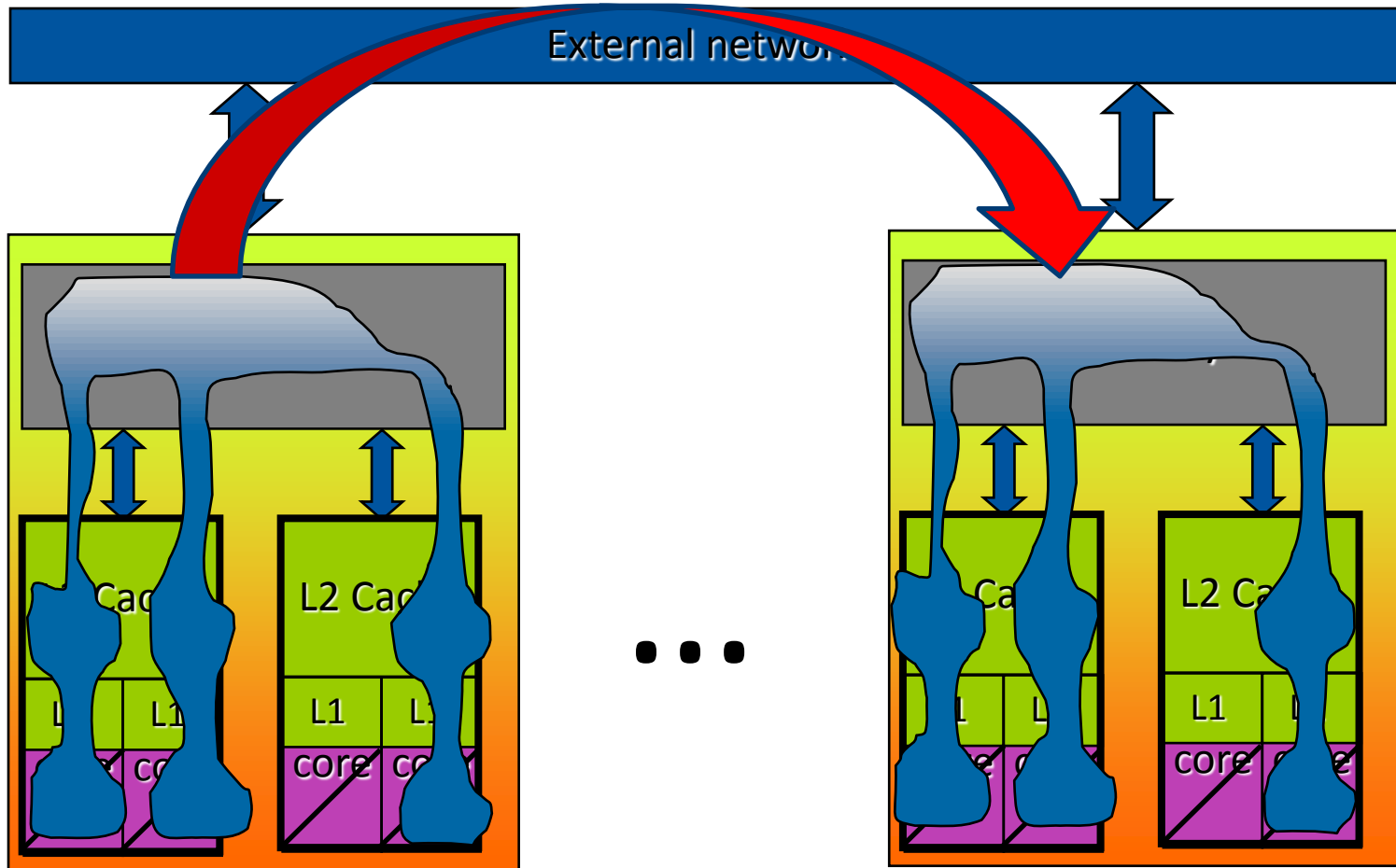
Typically it is the same binary, which is started on multiple processors.

(SPMD=single program multiple data paradigm)

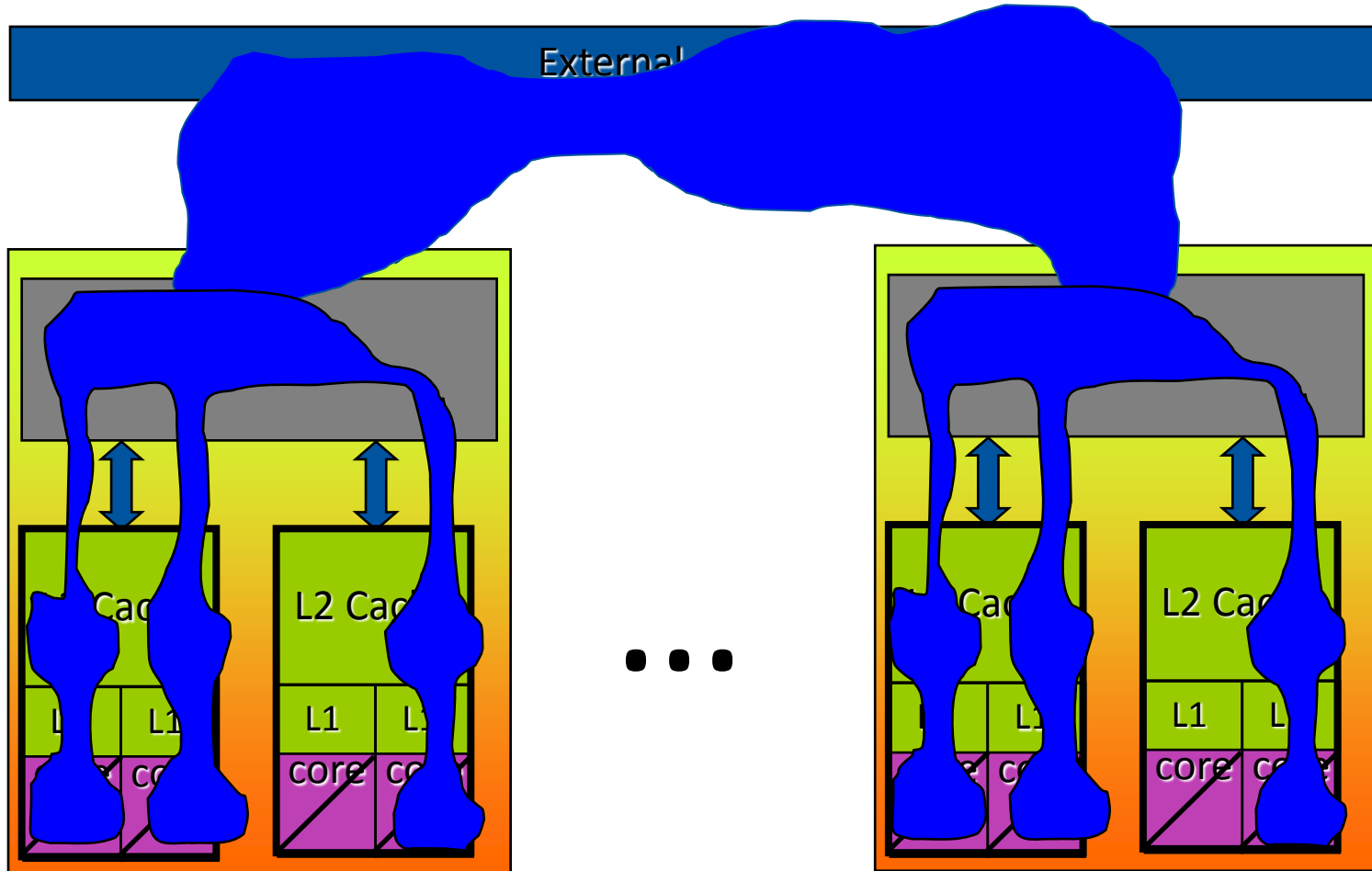




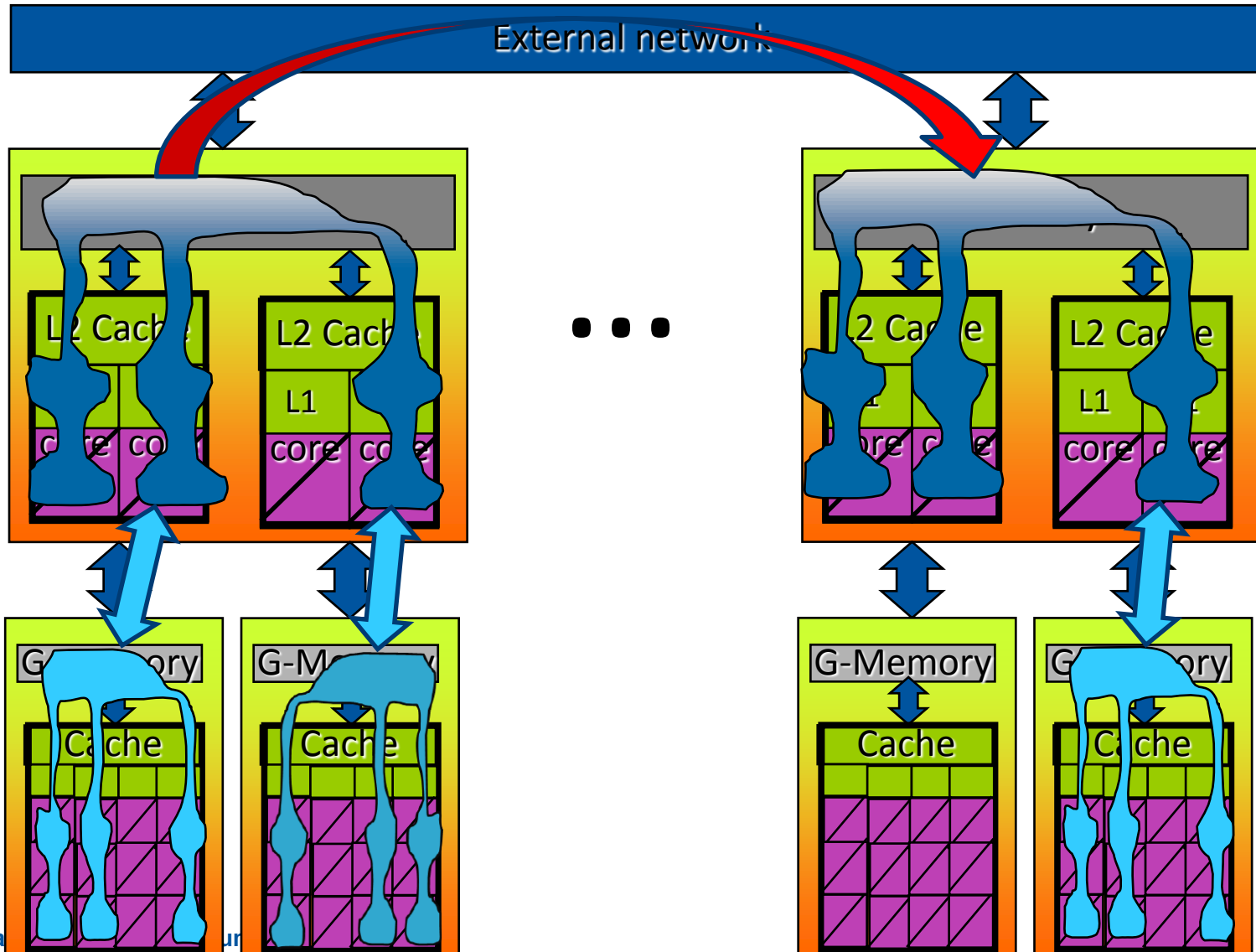
# MPI + OpenMP = Hybrid Parallelization



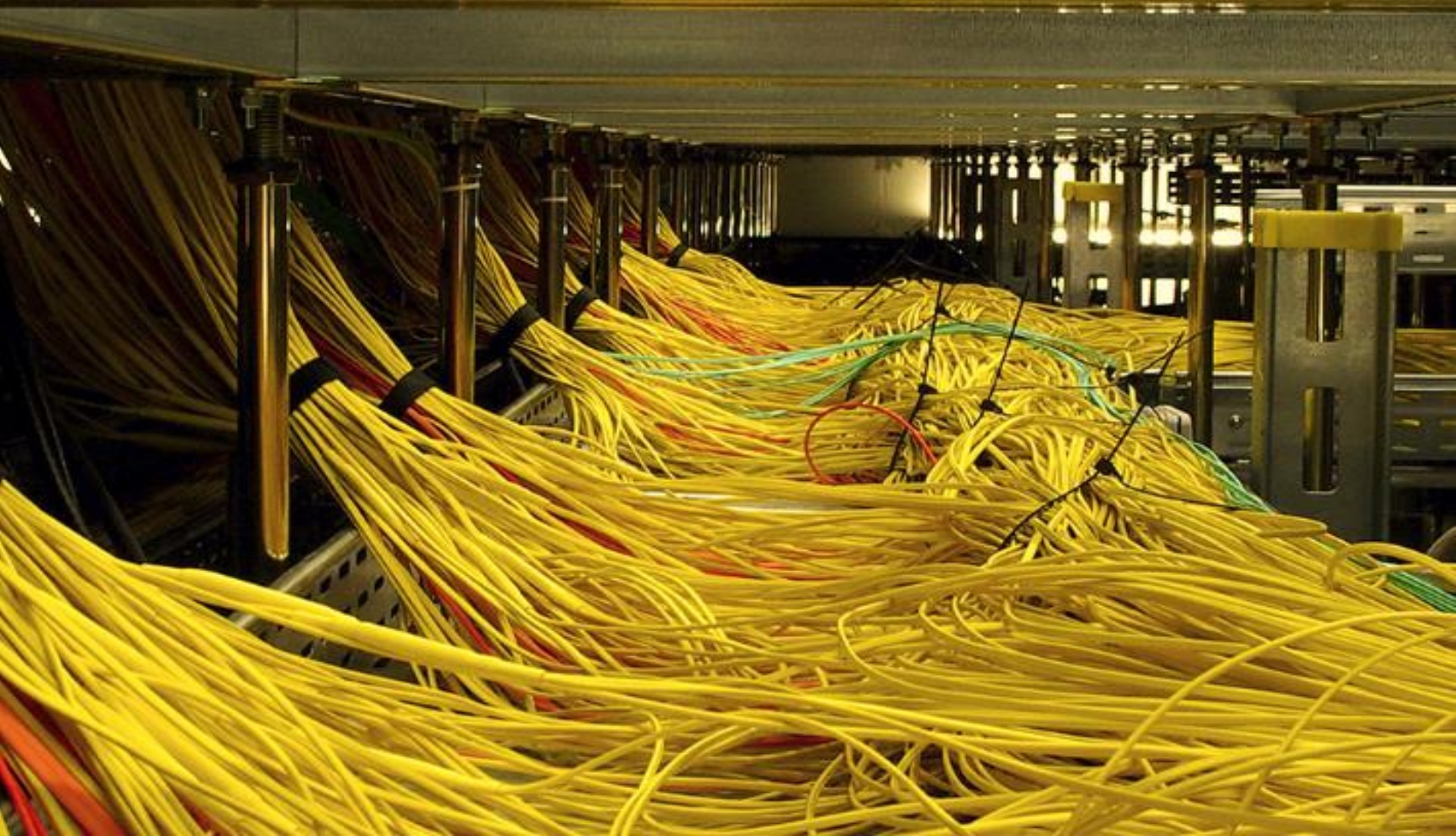
# Virtual Shared Memory Programming with OpenMP (using Software from ScaleMP)



and then there are Accelerators / Coprocessors  
( NVIDIA GPGPUs, Intel Xeon Phi) ...



# How to deal with this Complexity?



<b>Part I</b> Monday, July 29, 14:00-17:00	<b>Parallel Computing Architectures &amp; The RWTH Aachen Cluster Environment</b>
<b>Part II</b> Tuesday, July 30, 9:00-17:00	<b>Introduction to OpenMP Programming incl Labs</b>
<b>Part III</b> Wednesday, July 31, 9:00-17:00	<b>Advanced OpenMP Programming incl Labs</b>
<b>Part IV</b> Thursday, August 1, 9:00-17:00	<b>Basic message passing with MPI incl Labs</b>
<b>Part V</b> Friday, August 2, 9:00-15:30	<b>Advanced MPI, profiling and debugging of MPI applications incl Labs</b>

# Parallel Programming Summer Course 2013

## Agenda

	Monday, July 29	Tuesday, July 30	Wednesday, July 31	Thursday, August 01	Friday, August 02
<b>09:00 - 10:30</b>		Introduction to OpenMP Programming I (Christian Terboven)	Advanced OpenMP: Programming for Performance (Christian Terboven)	MPI: Parallel programming with message passing. Basic communication operations in MPI. (Hristo Iliev)	MPI: Hybrid programming. Often used parallel programming patterns. (Hristo Iliev)
<b>10:30 - 11:00</b>	break	break	break	break	break
<b>11:00- 12:30</b>		Lab Time	Lab Time	Lab Time	Lab Time
<b>12:30 - 14:00</b>	lunch break	lunch break	lunch break	lunch break	lunch break
<b>14:00 - 15:30</b>	Welcome (Dieter an Mey)	Introduction to OpenMP Programming II (Christian Terboven)	Advanced OpenMP: Tools (Dirk Schmidl)	MPI: Collective communication. User-defined datatypes. Virtual topologies. (Hristo Iliev)	MPI: Debugging and profiling of MPI applications. (Hristo Iliev)
	Parallel Computing Architectures (Christian Terboven)				Lab Time
<b>15:30 - 16:00</b>	break	break	break	break	break
<b>16:00 - 17:00</b>	Parallel Computing Architectures: Outlook (Christian Terboven)	Lab Time	Lab Time	Lab Time	
	The RWTH Aachen Cluster Environment (Tim Cramer)				



**Welcome to  
Parallel Programming  
Summer 2013**